Technology Scaling at an Inflexion Point: What Next? (FPGA Perspective)

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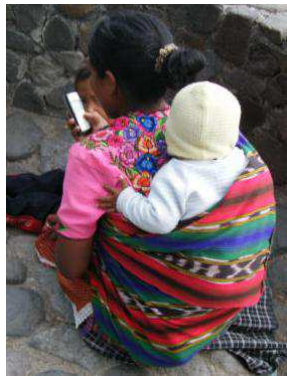
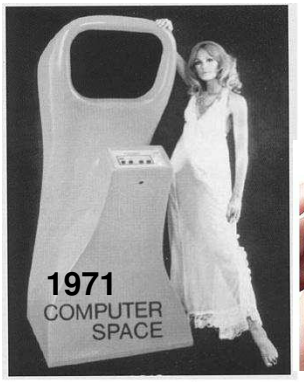
Scaling today: still healthy?

The positives

- Technology scaling continues!
  - almost 45 years after original formulation of Moore's Law (April 1965)
- The 2 year cycle of Moore's Law has become self-fulfilling
  - Industry still moving forward to 32nm & beyond
- Semiconductors are pervasive throughout society
  - $247 billion revenue in 2008
- Transistor counts > 1 billion in many leading edge products

THEN NOW





Warning signs for the future

- The costs of technology scaling are increasing every generation
  - Industry move to the fabless / foundry model
  - Foundry industry consolidation, development consortia, etc.
- IC development costs beyond the reach of most
  - $60M chip development cost at 45nm
  - ASIC design starts disappearing (except for a few high volume products)
- Lithography, the enabler of scaling, under severe pressure
  - Next gen. lithography platforms (EUV, E-Beam) not viable yet
- Approaching the limits of the MOSFET
  - Fundamental sub-threshold swing & design headroom limits Vt & Vcc scaling

Looking forward

Technology scaling will continue for many years!

- New lithography solutions are in development
  - Meanwhile double patterning will tide us over
- However, there will be no new 'miracle device' for many years
  - Devices demonstrated to beat kT/q, but not ready for prime time yet
  - Until then, designers will just have to live with the MOSFET – it still has an On/Off ratio > 10^6

Just a few companies moving ahead with most advanced technologies

- Only 3 companies to spend > $1B CapEx in 2009 (FabTech Aug '09)
  - Continued consolidation in foundry space; further moves to fablite & fabless model

The 'Programmable Imperative'

- Majority of design starts moving from ASICs to FPGAs
  - Mandated by business conditions (risk & TTM)
  - Enabled by increasing capability, density & performance of leading edge FPGAs

'More than Moore': 3D technology etc.

- System level integration beyond the single chip SoC
  - High bandwidth processor / memory; optical / high performance IO etc.

What should the ICDesigner worry about?

- 1st time right design: cannot afford to spin an ASIC design (use FPGA's!)
- Power: circuit solutions to minimise power wastage (clock & power gating etc.)
- Headroom: continuing squeeze on (Vcc - Vt): every 5mV costs > 1% in performance
- Variability & 3D effects: extensive simulation work will be required

What if Moore's Law had followed a 3 year cycle?

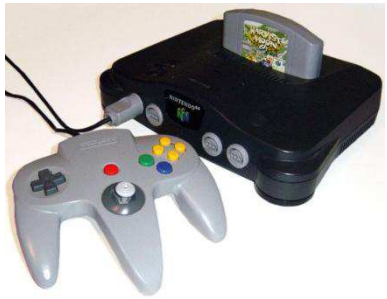
Instead of addressing the challenges of 32nm we would be looking at 0.25um

- Turn the clock back to 1999….
- Largest chips: Pentium III; Virtex XCV1000 FPGA; etc.
- Just 10 million transistors…

You would not be worrying so much about scaling, power, variability, etc!

BUT: our kids would still be playing video games & you would not be able to check your email as we sit here….

Nokia



Nintendo 64

In conclusion: no technical 'inflexion point' for at least 5-10 years; yet perhaps a financial/business one: only a few companies can afford to continue!

THANK YOU!

Appendix

Background: Moore's Law & Scaling

- *Original formulation in Electronics Magazine April 1965: "The complexity for minimum component costs has increased at a rate of roughly a factor of two per year ... Certainly over the short term this rate can be expected to continue, if not to increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe it will not remain nearly constant for at least 10 years. That means by 1975, the number of components per integrated circuit for minimum cost will be 65,000. I believe that such a large circuit can be built on a single wafer"*
- *In 1975, Moore altered his projection to a doubling of transistor count every two years*